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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,310	12/05/2003	Yoshinao Morikawa	559502000600	1372

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EXAMINER	
LE, THONG QUOC	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/729,310	MORIKAWA, YOSHINAO	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-6 are presented for examination.

Information Disclosure Statement

2. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 01/15/2004.

3. Information disclosed and list on PTO 1449 was considered.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting

directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamada (U.S. Patent No. 6,822,895).

Regarding claim 1, Yamada discloses a nonvolatile semiconductor memory device (Figure 1) comprising:

a memory cell array (Figure 1, 52) constituted by arranging a plurality of nonvolatile memory cells in a row direction and a column direction respectively and arranging the plurality of word lines (WL) and the plurality of bit lines (BL) in the row direction and the column direction respectively in order to select a predetermined memory cell or a memory cell group out of the arranged nonvolatile memory cells (Figure 1, Column 7, lines 42-48);

wherein the memory cells are respectively constituted by connecting one end of a variable resistive element (4) for storing information in accordance with a change of electrical resistances with the source of a selection transistor (Figure 1, 5), and

in the memory cell array, the drain of the selection transistor is connected with a common bit line along the column direction, the other end of the variable resistive element is connected with a source line, and the gate of the selection transistor is connected with the common word line along the row direction (memory cell 52 includes transistor 5 and resistor 4 and connection clarity as present claim invention).

Regarding claims 2-3, Yamada discloses wherein the variable resistive element is a variable resistive element whose electrical resistances are changed due to an electrical stress (Column 7, lines 32-41), and wherein the variable resistive element is formed by a perovskite structural oxide containing manganese (Column 1, lines 24-57).

7. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamada (U.S. Patent No. 6,760,244).

Regarding claim 1-6, Yamada discloses a nonvolatile semiconductor memory device (Figure 1) comprising: a memory cell array (Figure 1) constituted by arranging the plurality of nonvolatile memory cells (52) in a row direction and a column direction respectively and arranging the plurality of word lines (WL) and the plurality of bit lines (BL) in the row direction and the column direction respectively in order to select a predetermined memory cell or a memory cell group out of the arranged nonvolatile memory cells; wherein the memory cells are respectively constituted by connecting one end of a variable resistive element (4a) for storing information in accordance with a change of electrical resistances with the source of a first selection transistor (5a) and moreover connecting the other end of the variable resistive element with the drain of a second selection transistor (5b) , and in the memory cell array, the drain of the first selection transistor is connected with the common bit line along the column direction, the source of the second selection transistor is connected with a source line, and gates of the first and second selection transistors are connected with the common word line along the row direction (Figures 1-3), and wherein the variable resistive element is a variable resistive element whose electrical resistances are changed due to an electrical

stress, and wherein the variable resistive element is formed by a perovskite-structural oxide containing manganese (Column 1, lines 25-65).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

THONG LE
PRIMARY EXAMINER